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<b>TRANSMITTAL OF RESPONSE</b>			Docket No. 3430-0131P
In re Application of: Kwang-Jo HWANG			
Application No. 09/648,111	Filing Date August 25, 2000	Examiner N. D. Richards	Group Art Unit 2815
Invention: METHOD OF PATTERNING A METAL LAYER IN A SEMICONDUCTOR DEVICE			
<p style="text-align: center;"><b><u>TO THE COMMISSIONER OF PATENTS:</u></b></p> <p>Transmitted herewith is a Response in this application, in response to the Notice of Non-Compliant Appeal Brief mailed August 17, 2006. This Response contains a revised Summary of Claimed Subject Matter in compliance with 37 C.F.R. 41.37.</p> <p>The fee for filing the Appeal Brief is <u>\$ 500.00</u> and was paid on June 20, 2006.</p> <p><input checked="" type="checkbox"/> Large Entity      <input type="checkbox"/> Small Entity</p> <p><input type="checkbox"/> A petition for extension of time is also enclosed.</p> <p>The fee for the extension of time is _____.</p> <p><input type="checkbox"/> A check in the amount of _____ is enclosed.</p> <p><input type="checkbox"/> Charge the amount of the fee to Deposit Account No. <u>02-2448</u>. This sheet is submitted in duplicate.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input checked="" type="checkbox"/> The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. <u>02-2448</u>. This sheet is submitted in duplicate.</p> <div style="display: flex; justify-content: space-between; align-items: flex-start;"><div style="width: 60%;"><p><i>Robert E. Chong #42,593</i> _____ Esther H. Chong Attorney Reg. No. : 40,953 BIRCH, STEWART, KOLASCH &amp; BIRCH, LLP 8110 Gatehouse Road Suite 100 East P.O. Box 747 Falls Church, Virginia 22040-0747 (703) 205-8000</p></div><div style="width: 35%; text-align: right;"><p>Dated: <u>September 15, 2006</u></p></div></div>			



MS APPEAL BRIEF - PATENTS  
PATENT  
3430-0131P

IN THE U.S. PATENT AND TRADEMARK OFFICE

In Re Application of

Before the Board of Appeals

Kwang-Jo Hwang

Appeal No.

Appl. No.: 09/648,111

Group: 2815

Filed: August 25, 2000

Examiner: N.D. Richards

Conf. No.: 5562

For: METHOD OF PATTERNING A METAL LAYER IN A  
SEMICONDUCTOR DEVICE

RESPONSE TO NOTIFICATION OF NON-COMPLIANT BRIEF  
(37 C.F.R. 41.37)

**MS APPEAL BRIEF- PATENTS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

September 15, 2006

Dear Sir:

In response to the Notice of Non-Compliant Appeal Brief mailed August 17, 2006, the applicant respectfully submits the appended Summary of Claimed Subject Matter in accordance with 37 C.F.R. 41.37. The appended Summary of Claimed Subject Matter contains a precise explanation of the subject matter defined in each of the independent claims involved in the appeal and refers to the figures by reference numeral.

A replacement Appeal Brief is not being filed pursuant to MPEP 1205.03, which states: "When the Office holds the brief to be defective solely due to appellant's failure to

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provide a summary of the claimed subject matter as required by 37 CFR 41.37 (c)(1)(v), an entire new brief need not, and should not, be filed. Rather, a paper providing a summary of the claimed subject matter as required by 37 CFR 41.37 (c)(1)(v) will suffice.”

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

September 15, 2006

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

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**APPENDIX: SUMMARY OF CLAIMED SUBJECT MATTER**

**V. SUMMARY OF CLAIMED SUBJECT MATTER**

**Claim 1:** As set forth in independent claim 1, the present invention pertains to a method of manufacturing a liquid crystal display device that includes forming a switching element on a substrate **31** (e.g., page 4, line 5 of the present specification); forming a passivation layer **37** over the substrate **31** (e.g., page 4, lines 5-6); depositing a metal layer **44** on the passivation layer **37** (e.g., page 5, line 6); forming a photoresist pattern **36** on a surface of the metal layer **44**, such that an upper portion of the metal layer is exposed (e.g., page 5, lines 7-8). The method also includes treating the exposed portion of the metal layer **44** with a first plasma, prior to any step of etching the photoresist pattern **36**, and prior to any step of etching the metal layer **44**, thereby lowering an internal binding force in the exposed portion of the metal layer **44** to increase the subsequent etch rate of the metal layer **44** (e.g., page 6, line 15 to page 7, line 8). Etching the treated portion of the metal layer forms a pixel electrode 39 (e.g., page 4, lines 9-10, page 7, lines 5-6). Also, the depositing of a metal layer **44** on the passivation layer **37**, forming a photoresist pattern **36**, and treating the exposed portion of the metal layer **44** are sequentially performed (e.g., page 6, lines 8-14). (Figures 5, 6A and 6B).

**Claim 22:** As set forth in independent claim 22, the present invention pertains to a method of patterning a metal layer **44** that includes the steps of depositing a metal layer **44** over a substrate **31** (page 3, line 15); forming a mask **36** on a surface of the metal layer **44** (page 3, line 15), leaving an upper portion of the metal layer **44** uncovered (page 3, line 16); exposing the uncovered portion of the metal layer **44** to a first plasma (page 3, lines 16-17), prior to any step of etching the metal layer **44**, thereby lowering an internal binding force (page 3, line 17) in the uncovered portion (page 3, line 17) to increase a

subsequent etch rate of the metal layer **44** (page 7, lines 4-8); and etching the uncovered portion of the metal layer **44** with a second plasma to form a metal pattern (page 3, lines 18-19), wherein the depositing a metal layer **44** over a substrate **31**, forming a mask **36** on a surface of the metal layer **44**, and exposing the uncovered portion of the metal layer **44** are sequentially performed (Page 6, lines 8-21). (Figures 5, 6A and 6B).

**Claim 30:** As set forth in independent claim 30, the present invention pertains to a method manufacturing a pixel electrode in a liquid crystal display device that includes the steps of depositing a metal layer **44** on a passivation layer **37** which partially covers a transistor **32, 34, 35** (page 3, lines 21-22); forming a photoresist pattern **36** on a surface of the metal layer **44**, leaving an upper portion of the metal layer **44** uncovered (page 3, lines 22-23); exposing the uncovered portion of the metal layer **44** to at least one first gas (page 3, line 23 to page 4, line 1), prior to any step of etching the photoresist pattern **36** and prior to any step of etching the metal layer **44** (page 7, lines 2-5), to lower an internal binding force in the uncovered portion to increase a subsequent etch rate of the metal layer **44** (page 7, lines 4-8); and etching the uncovered portion of the metal layer **44** with at least one second gas to form a pixel electrode **39** (page 7, lines 4-5), wherein the depositing a metal layer on the passivation layer **37**, forming a photoresist pattern **36**, and exposing the uncovered portion of the metal layer **44** are sequentially performed (Page 6, lines 8-21). (Figures 5, 6A and 6B).

**Claim 31:** As set forth in independent claim 31, the present invention pertains to a method of manufacturing a pixel electrode **39** in a liquid crystal display device that includes the steps of depositing a metal layer **44** on a passivation layer **37** which partially covers a transistor **32, 34, 35** (page 3, lines 21-22); forming a photoresist pattern **36** on a

surface of the metal layer **44**, leaving an upper portion of the metal layer **44** uncovered (page 3, lines 22-23); exposing the uncovered portion of the metal layer **44** to at least one first gas (page 3, line 23 to page 4, line 1), prior to any step of etching, to lower an internal binding force in the uncovered portion to increase a subsequent etch rate of the metal layer **44** (page 7, lines 4-8); and etching the uncovered portion of the metal layer **44** with at least one second gas to form a pixel electrode **36** (page 7, lines 4-5, wherein the depositing a metal layer **44** on the passivation layer **37**, forming a photoresist pattern **36**, and exposing the uncovered portion of the metal layer **44** are sequentially performed (Page 6, lines 8-21). (Figures 5, 6A and 6B).